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L1Track/FTK++ Processing

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My experience

- Kersten Distinguished Service Professor, University of Chicago
- A leader of the trigger hardware project for the CDF experiment at Fermilab (initial system and upgrades).
- Co-spokesperson of CDF at the time of the discovery of the top quark.
- One of the leaders of the original project using the technology chosen for L1Track/FTK++: SVT in the CDF experiment
- ATLAS FTK Project Leader from its inception to 2014. Deputy Project Leader since then.
- PI of the NSF MRI grant for building FTK.

Outline

- The physics challenges
- The solution – hardware track finding
- Needed R&D
- US institute involvement
  - Current FTK involvement & NSF role
- Closing Remarks

Physics Challenges

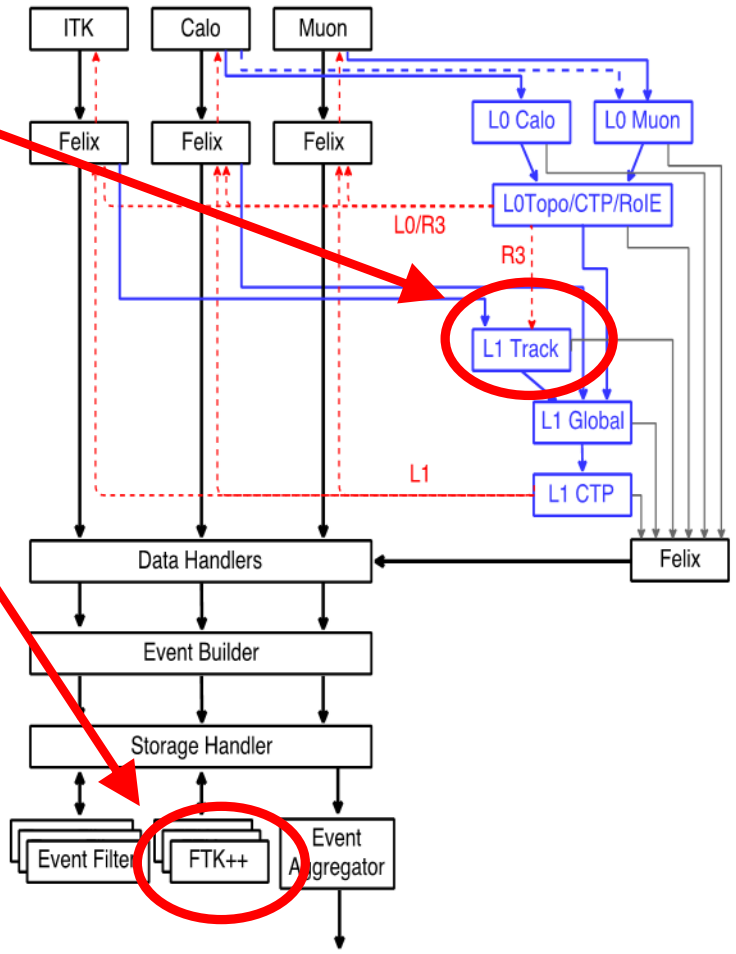
- The trigger uses partial detector information to select in real time those collisions with the greatest physics potential.
- At present, information from the calorimeter and muon systems are primarily used to make the decision. Since track reconstruction is computationally very intensive, it can only be done in small regions of the detector.
- At HL-LHC luminosities:
  - Physics needs $\Rightarrow$ maintain low energy thresholds
  - Large number of simultaneous collisions $\Rightarrow$ greater background rejection
- The solution requires more intensive use of track reconstruction.

Need for tracking in the trigger

- Level-1 trigger (L1Track):
  - Electron identification
  - Tau lepton selection
  - Ensuring that multiple objects originate in the same collision
- High-level trigger (FTK++):
  - Heavy quark (*b*) jet identification and rejection of light quark background
  - Tau lepton identification and rejection of light quark background
  - Improved resolution for the missing energy from the primary interaction
  - Increasing multi *b*-jet efficiency by going below the level-1 threshold for some of the *b*-jets
  - Determining the location of the primary collision (provides sharper turn-on curves)

Hardware track finding

- L1Track – regional tracking for the full 1 MHz level-0 event rate.
- FTK++ - global tracking for 100 kHz of the level-1 event rate.
- The hardware of the two systems is expected to be nearly identical.

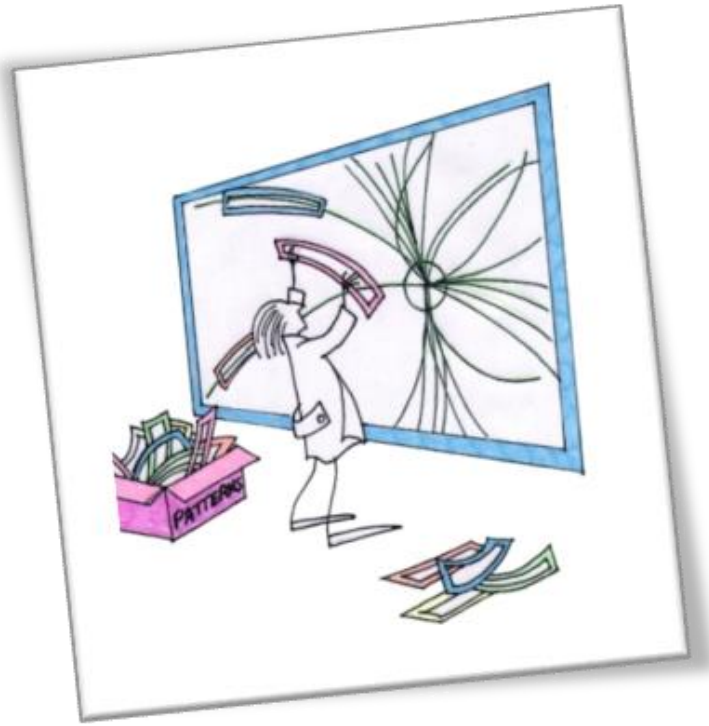


Hardware solution

- The small latency for global track reconstruction (< 100 μs, a factor > 10^3 faster than in a standard computer) is accomplished by using two “tricks”, one each for pattern recognition and track fitting.

Pattern recognition

- Massive parallelism is employed. In FTK, 1 billion track patterns are tested simultaneously.
- The Associative Memory ASIC chip (AM) is a HEP-specific content addressable memory (CAM):
  - Load a full event (8 Si layers in parallel)
  - Output patterns with hits on more than a programmable number of layers.
  - Essentially by the time the silicon hits are off detector, pattern recognition is done.
  - Current chip (AM06): 128k patterns (8000 AM chips in FTK)



Track fitting

- Normally, a fit of the hits to a helix is done – very time consuming.
- We found that in a small region of the detector the fit can be replaced by a linear calculation, with the resulting track parameter resolution nearly as good as a full fit.

$$p_i = \sum_j C_{ij} \cdot x_j + q_i$$

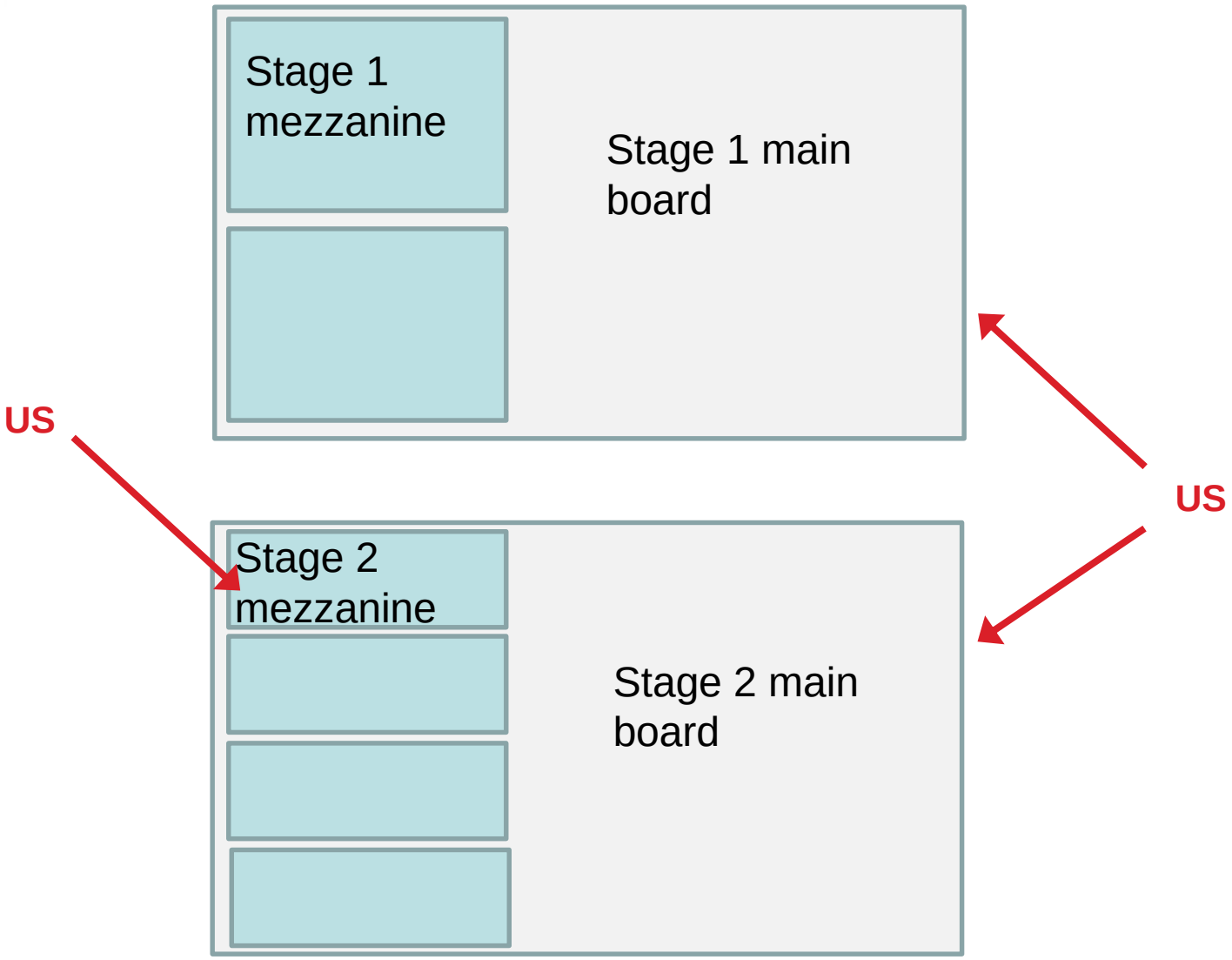
p_i : track parameters and components of the goodness of fit

x_j : measured hit position in each detector layer

C_{ij} and q_i : prestored constants

- Such a calculation is very fast in modern FPGA DSPs.
- In FTK, we do approximately 1 “fit” per nanosecond in each of the 512 FPGAs in the system.

L1Track/FTK++ two-stage processing



Stage 1

- Main board (US) receives hits from each of 8 detector layers.
- ATCA full-mesh backplane distributes hits to other main boards that need them (in the geometric coverage of the board, including the needed overlap).
- Hits are transferred to mezzanines.
- Mezzanine does pattern recognition (AM chips) and 1st stage fitting (goodness of fit only).
- Track candidates with good χ^2 are collected in the main board and sent to stage 2.

Stage 2

- Stage-2 main board (US) receives track candidates from stage-1 main board and hits from the detector layers not used in stage 1.
- ATCA full-mesh backplane distributes hits from the added layers to other main boards that need them.
- Hits and stage-1 tracks are transferred to mezzanines (US).
- Hits in the additional layers that are in the track candidate road are found and a fit is done using all layers. The goodness of fit and all of the track parameters are calculated. Tracks are kept that have an acceptable goodness of fit.
- Duplicate tracks are removed if they share more than a programmable number of hits in common.
- The tracks that remain are sent to the level-1 or HLT trigger.

Requirements

- L1Track
  - Process Regions of Interest (~ 10% of an event) for full 1 MHz level-0 event rate.
  - Tracks with $p_T > 4$ GeV/c
  - Reconstruction efficiency > 95% relative to offline reconstruction
  - Latency < 20 μs
- FTK++
  - Process full events (global tracking) for 100 kHz of the level-1 event rate.
  - Tracks with $p_T > 1$ GeV/c
  - Reconstruction efficiency > 95% relative to offline reconstruction
  - Latency ~ 100 μs

Needed R&D

- US responsibility: main board and 2nd-stage mezzanine
- Main board
  - Extrapolating from high luminosity data and using the final design of the new tracking detector and DAQ structure, determine the number of high speed links.
  - Choose the FPGA (cost vs. I/O ports and speed)
  - Partial prototypes to test data transfer on board, across ATCA backplane, to the RTM, and to the mezzanine.
- Mezzanine
  - Determine the required number of high speed links and fits/second.
  - Choose the FPGA (cost vs. number of fits per second) and external memory (speed and capacity)
  - Partial prototypes to test speed and critical functionality

US institutes

- Chicago
- Illinois
- Indiana
- Northern Illinois
- Pennsylvania
- Stanford

- Reminder: The largest fraction of the FTK funding came from the US (~50%), all provided by the NSF.

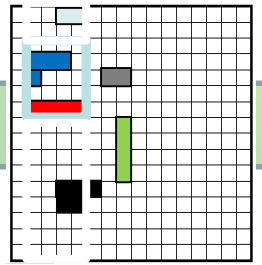
Group experience in FTK

Chicago

Input transmission

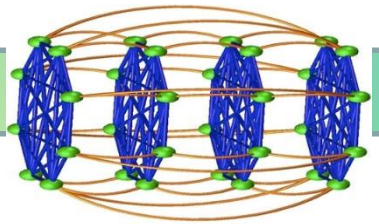
Japan, Europe

Custom pixel clustering algorithm on FPGAs

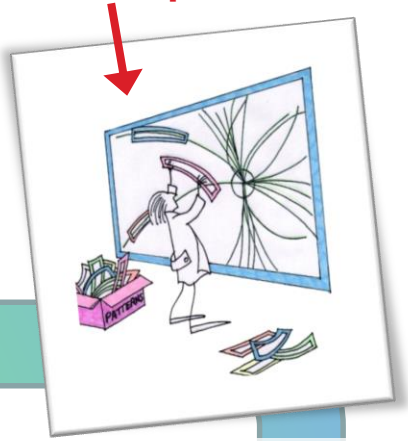


Stanford

The data is geometrically distributed to the processing units.

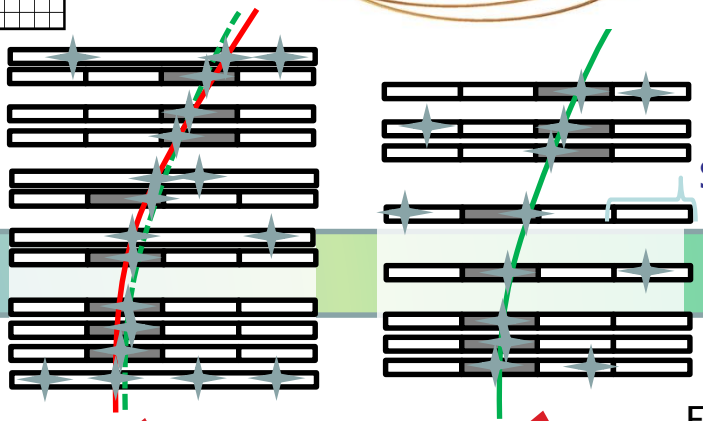


Europe



AM Pattern matching 8 layers: Hits compared at reduced resolution.

SS



Output preparation

Argonne

Illinois

Chicago

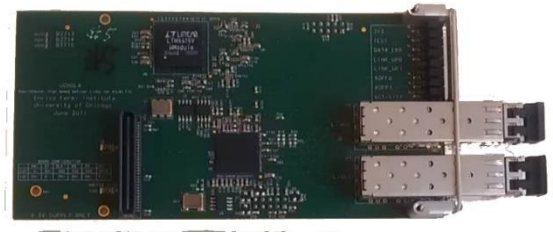
Full hits precision retrieved for good roads.
Fits reduced to scalar products.

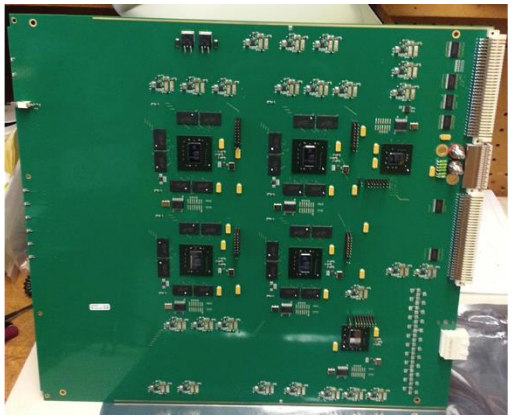
Closing Remarks

- Effective triggering in the HL-LHC era requires rapid track reconstruction.
- L1Track/FTK++ provides this using a proven technology.
- The US has a great deal of experience with this technology, both with the CDF SVT and the ATLAS FTK.
- The NSF has provided the bulk of the funding for both systems.
- There is a group of US institutions with talented physicist and engineering personnel that will design and build the US portion of the system.

Backup

FTK boards built in the US





Cost estimation

- Based on:
  - the expected data flow at HL-LHC luminosities
  - the cost of the US FTK boards that have been built
    - FTK Data Formatter → Main Board
    - FTK AUX & SSB → 2nd-stage mezzanine
  - an estimate of the improvement in cost and performance of FPGAs over the next 4 years
  - the number of patterns expected in the next generation of pattern recognition ASIC chips (AM)